

October 24, 2003

To: Commissioner for Patents

P.O.Box 1450

Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572

28 Davis Avenue

Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/628,913 07/29/03

Yeen Tat Chan et al.

METHOD OF FORMING A PARTIALLY DEPLETED SILICON ON INSULATOR (PDSOI) TRANSISTOR WITH A PAD LOCK BODY EXTENSION

| Grp. Art Unit:

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 77, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

CS-02-068

- U.S. Patent 6,537,861 to Kroell et al., "SOI Transistor with Body Contact and Method of Forming Same," describes a PDSOI with a body isolation trench.
- U.S. Patent 5,405,795 to Beyer et al., "Method of Forming a SOI Transistor Having a Self-Aligned Body Contact," discloses a SOI transistor with a self-aligned body contact.
- U.S. Patent 6,521,959 to Kim et al., "SOI Semiconductor Integrated Circuit for Eliminating Floating Body Effects in SOI MOSFETs and Method of Fabricating the Same," discloses a body extension and a body insulator.
- U.S. Patent 5,145,802 to Tyson et al., "Method of Making SOI Circuit with Buried Connectors," teaches a buried body tie to remove the danger of a parasitic transistor.

Sincerely

Stephen B. Ackerman,

Reg. No. 37761

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